IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 6, 7 and 12 in accordance with the following:

1. **(Currently Amended)** A thin film transistor (TFT) comprising ~~a lightly doped drain (LDD) region or~~an offset region having no doping and a plurality of primary crystal grain boundaries, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are ~~positioned in channel, source and drain regions but~~ not positioned in the ~~LDD or~~ offset region, and wherein a width of the ~~LDD region or~~ offset region, included in an activation layer, is ~~shorter~~smaller than a distance between the primary crystal grain boundaries.

2. **(Cancelled)**

3. **(Original)** The thin film transistor according to claim 1, wherein the polysilicon substrate is formed by a sequential lateral solidification (SLS) method.

4. **(Original)** The thin film transistor according to claim 1, wherein the thin film transistor is used in an LCD (liquid crystal display) or organic EL (electroluminescent) device.

5. **(Previously Presented)** The thin film transistor according to claim 1, wherein the primary crystal grain boundaries are perpendicular to a current direction between source and drain regions of the thin film transistor.

6. **(Currently Amended)** A thin film transistor (TFT) comprising a lightly doped drain (LDD) region or offset region and a plurality of primary crystal grain boundaries, wherein the thin film transistor is formed so that the primary crystal grain boundaries of a

polysilicon substrate are positioned in channel, source and drain regions but not positioned in the LDD or offset region, and wherein a width of the LDD region or offset region is less than a distance between two adjoining primary crystal grain boundaries~~the primary crystal grain boundaries are inclined to a current direction between active source and drain regions of the thin film transistor at an angle of $-45° \leq \Theta \leq 45°$~~.

7. **(Currently Amended)** A flat panel display device comprising:

a thin film transistor comprising:

~~a lightly doped drain (LDD) region or~~an offset region having no doping, and a plurality of primary crystal grain boundaries,

wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are ~~positioned in channel, source and drain regions but~~ not positioned in the ~~LDD or~~ offset region, and wherein a width of the ~~LDD region or~~ offset region, included in an activation layer, is ~~shorter~~smaller than a distance between the primary crystal grain boundaries.

8. **(Cancelled)**

9. **(Original)** The flat panel display device according to claim 7, wherein the polysilicon substrate is formed by a sequential lateral solidification (SLS) method.

10. **(Original)** The flat panel display device according to claim 7, wherein the thin film transistor is used in an LCD (liquid crystal display) or organic EL (electroluminescent) device.

11. **(Previously Presented)** The flat panel display device according to claim 7, wherein the primary crystal grain boundaries are perpendicular to a current direction between source and drain regions of the thin film transistor.

12. **(Currently Amended)** A flat panel display device comprising:

a thin film transistor comprising:

a light doped drain (LDD) region or offset region, and a plurality of primary crystal grain boundaries,

wherein the thin film transistor is formed so that the primary crystal grain boundaries of a polysilicon substrate are positioned in channel, source and drain regions but not positioned in the LDD or offset region, and

wherein a width of the LDD region or offset region is less than a distance between two adjoining primary crystal grain boundaries~~the primary crystal grain boundaries are inclined to a current direction between source and drain regions of the thin film transistor at an angle of $-45° \leq \Theta \leq 45°$~~.

13 - 14. **(Cancelled)**